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Active Quenching of Geiger Muller detectors based on FPGA

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ABSTRACT

An important parameter of Geiger-Muller detectors is their lengthy dead time, which causes a nonlinear response at high counting rates. The dead time depends on the detector's characteristics (size, geometry and material) and its connected electronics (detection, counting, and quenching circuits) as well as the detection settings. A highly effective method for dead time cancellation is the time-to-first-count method, though it requires a complex electronic circuitry for active quenching of the Geiger-Muller detector. In this paper, we present the development of a fast and efficient active quenching circuit based on FPGA technology. Additionally, the system architecture simultaneously acquires the time to first count (referred to as time intervals in this paper).The system achieves a time resolution of 10 ns, which is sufficient for Geiger-Muller detectors given their timing characteristics, with dead times ranging from several microseconds to over 200 microseconds. The ZP1210 Geiger-Muller detector, which has a dead time of approximately 200 µs according to the manufacturer's datasheet, is used as a case study. The dead time of the detector is about 200 µs according to the manufacturer datasheet. This active quenching circuit which is implemented on a FPGA, is experimentally tested on this detector. Details of the work are explained in the text.

Keywords: Geiger-muller detector; Active quenching circuit; FPGA programming; Dead time.

1. Introductions

It has been about a century since Geiger-Muller detectors were introduced. These detectors have been utilized in various applications, including nuclear reactor instrumentations, oil industry, and space and submarine investigations. Different designs of the detector have been developed to detect various particles (alpha, beta, and gamma) [1,2].

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Historically, efforts to develop and improve the performance of Geiger-Muller detector performance, began with the aim of enhancing the speed control of the tube operation. This started eight years after the detector's invention, when Neher used high-speed semi-electronic circuits in 1936, with further revisions in 1938.. Subsequently, Getting and Ruark employed multi-vibrators as high-speed electronic circuits in 1937 and 1938 [3].

Simultaneously with the growth and development of electronic circuits for this type of radiation detector, various methods for calculating and measuring the dead time to estimate the Geiger-Muller discharge interval were investigated [4].

Two ideal dead time models, paralyzable and non-paralyzable, were introduced by Feller and Evans from 1955 to 1988 [3]. Subsequently,Tax derived the hybrid model using the Laplace transfer function and continued refine it until 1988 [5]. New hybrid models of dead time in the Geiger-Muller detector were presented by Gardner and Lee in 2000 [5]. Finally, a new phenomenological model for the Geiger-Muller detector dead time was introduced by Osman et al. in 2017 [6].

Although the use of these dead time correction models significantly expands the operational range of existing detectors [3], further research demonstrated that employing active quenching circuits and, consequently,reducing the consumption of internal quenching gas , directly increases the device's lifetime and efficiency. The first example of such circuits was presented by Meyer in 1948 [2] and further developed by Crowell in 1958 [7]. Matthews adapted it to a two-transistor circuit in 1969 [8] which was then improved again in 1986 [9]. To optimize the Geiger-Muller detector for specific and long-term measurements and to reduce failure, especially in challenging and complex conditions requiring extended timing, a new active quenching circuit was designed by Vagle et al. (2007 and 2009) again. This model was subsequently used in review studies by Usman et al. in 2018 [10,11].

Based onthe history mentioned above and the purpose of this study, one of the most important parameters of Geiger-Muller detectors is the dead time. Dependingon the size and geometry of the detector, dead time ranges from 20 to 300 microseconds. The high for the ionization process and avalanche production throughout the detector. Traditionally, the quenching of the avalanche is performed by an additive gas. However, quenching one avalanche consumes one atom of the additive gas. That is why the lifetime of Geiger Muller detectors is limited [12].

Using an active quenching circuit, the limited lifetime of Geiger-Muller detectors is extended. Additionally, the time-to-first count method can be implemented to decrease the detector's dead time [1]. In the present paper, the active quenching circuit and the time-to-first count method are efficiently implemented based on FPGA using the system architecture.

Among all the features, applications, and advantages of FPGA, the factors that made its use particularly important in this study are the implementation of very complex functions, high processing speed, reduction of required hardware, simple and standard programming, fast testing of the circuit, affordability, especially in low-volume productions, user programmability, the ability to define several processing cores, and multitasking capabilities, parallel processing capability, elimination of noise caused by different and separate parts in the circuit, and a 100% safety factor due to the impossibility of accessing its internal content [13,14].

In the digital system of this study, a discrete time interval of 10 ns is used. The ZP1210 Geiger-Muller detector is chosen as a case study, and experimental investigations are performed.

2. Material and methods

The Geiger-Müller ZP1210 detector (Centronic Co., which operates at a high voltage of about 450V and has a dead time of 200μs) used in this study had its lifespan and efficiency improved by using an active quenching circuit and correcting the dead time [15].

The active quenching circuit includes a MOSFET transistor switch, and a level translator circuit (as shown in Fig. 1). In this configuration, the MOSFET switch, and through the ground connection of its source pin, electrically connects the resistive connection to the drain to the ground, ultimately creatinga resistance division in the Geiger-Muller anode head.

This causes the voltage to split, resulting in a Geiger-Muller voltage of less than 450 volts, as well as the threshold voltage required for an avalanche to occur, causing the detector to shut down and the avalanche to stop. The MOSFET switches on and off with two voltages, 0 and 15 volts, while the threshold value of this switch is less than 15 volts. This setting can speed up the switching time at higher voltage and improve its performance.

A level translator circuit with a range of 0 to 3.3 volts takes Low Voltage TTL (LVTTL) signals from the FPGA and converts them to 0 and 15 volts to control the MOSFET transistor switch. Turning the switch on and off through the resistor split connected to it can raise the voltage above and below the detector threshold. Under these conditions, the avalanche event can be actively controlled [16,17].

The other part of this circuit is the non-inverting operational amplifier (TL081CP), which has a significant gain factor. It has high input impedanceand a closed-loop gain of more than one. In the design, it acts as a buffer and amplifier. The output signal of this Op Amp has a descending exponential shape with a range between 0 and 10 volts (as shown in Fig. 1). When the switch is inactive, the detected pulse is displayed, and when the switch is active, this pulse decreases faster. In general, if the quenching circuit were not active, this sequence would be more than 100μs which, despite this circuit, would have been slower.

The detector pulse then enters the Schmitt trigger 4016 comparator circuit. Its comparison voltage is approximately 3.5 volts. If the input value is greater than the breakdown voltage, the output is high, if it is smaller, the output becomes low. Thus, a cleaner pulse with a voltage of 3.3 volts is shaped for injection into the FPGA. When Geiger-Muller detector detects radiation, a pulse is observed at the detector's output, which is then fed to the FPGA. This detection pulse turns the switch on or the high voltage source off until the avalanche stops.

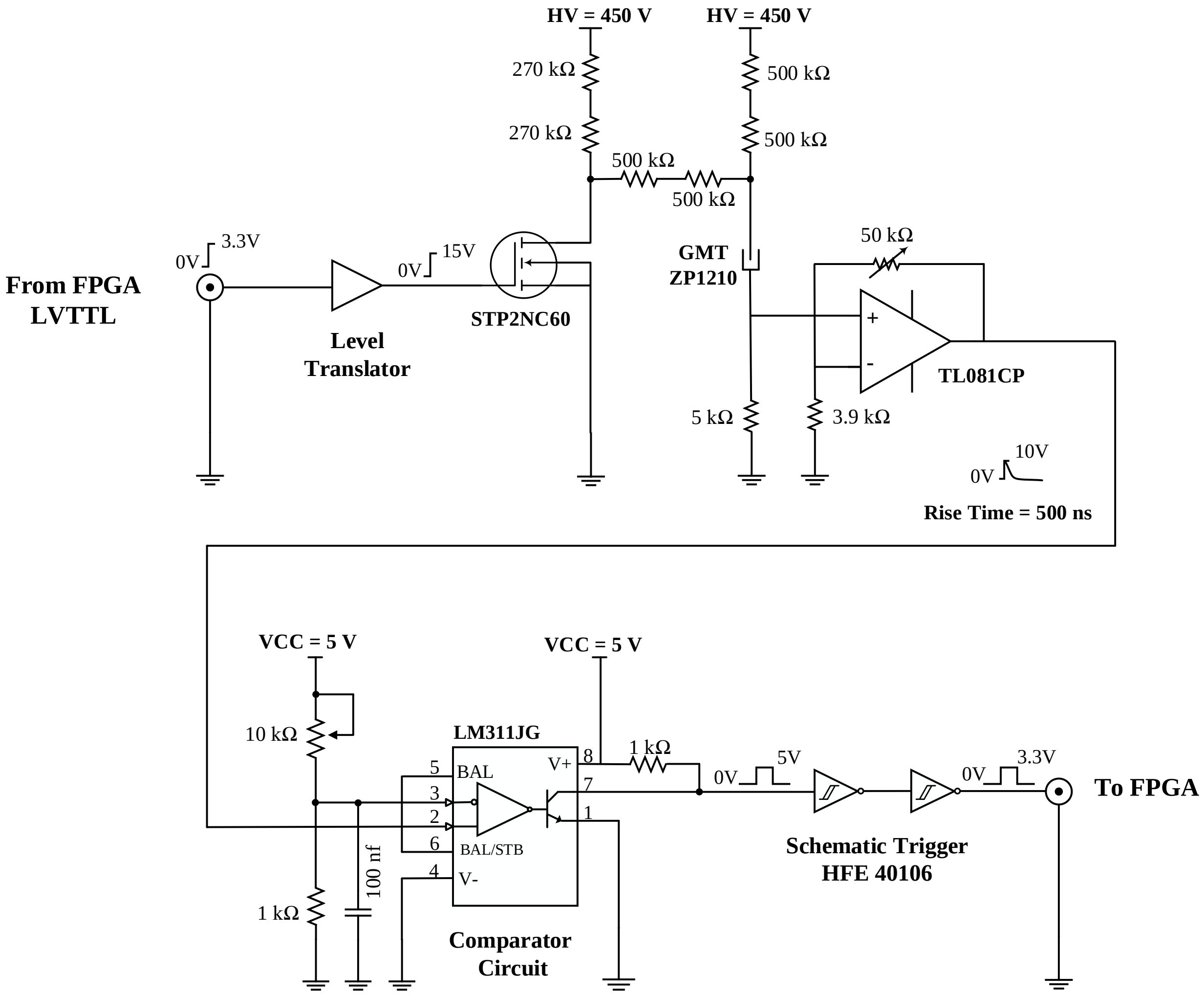

Fig. 1. Active quenching circuit designed for the Geiger-Muller detector model ZP1210.

The designed FPGA board includes an FPGA chip (as the core) and a series of external SRAM memory banks (to provide sufficient memory space for the data acquisition). In this design, oscillating crystals with a frequency of 100MHz are used to discretize the time. Thus, a time step of 10 nanoseconds is achieved, which enters the PLL[1] part. PLLs capture the desired frequency and generate other frequencies with various phase differences.

Here, as a stabilizer, it performs frequency reconstruction and delivers the same 100MHz input. As in other digital systems, in discrete time measurements, the higher the frequency, the higher the temporal resolution.

As shown in Fig. 2, the resulting frequency is input into the synchronization block to synchronize the detector signal. This block does not have a time connection with the 100MHz frequency. Its output is usually low unless the clock pulse and detector pulse are simultaneously high, in which case the input transmitted to the output. In other words, input changes are updated by the 100 MHz clock at the output.

Next, the timing VHDL Code block picks up the pulse, and the counter starts counting.

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[1] Phase Lock Loop

Simultaneously, the pulse commands the high voltage to turn on, the switch goes off, and the counter activates, waiting for the next pulse to be detected. When the pulse arrives, it reads the counter value and the VHDL code and then stores this information in FIFO memory.

When the switch turns on again, the high voltage source turns off for a few microseconds, awaiting the next pulse. During this time interval, the counter counts and the VHDL code reads the count. The switch turns on again, and the high voltage source turns off for a few microseconds, awaitingthe next pulse. Again, the counter counts this time interval, and the VHDL code reads the count. The switch turns on again and the high voltage source turns off for a few microseconds, awaiting the next pulse. The counter counts the time intervals again, and the data is read by the VHDL code. In summary, the high voltage switch turns off (goes high), and the counter activates, waiting for the detected pulse. During this time interval, the timing VHDL code block reads the counter valueand pushes it into the FIFO memory, clearing the Count Enable signal and deactivating the counting activator signal. After clearing the counter, it reactivates the counter, raises the high voltage, waits for the next pulse, reads the counter value when the next pulse arrives, and pushes it into the FIFO memory.

The VHDL code reads the time interval between the pulses, which is the same number as the counter and continuously stores it in FIFO memory. It measures the time interval preciselywhen the high voltage value is high until the detection pulse arrives.

As shown in Fig. 2, the NIOS processor connects to FIFO memory, PC, and external SRAM memory. This processor reads and pushes a number into SRAM memory after detecting it in the FIFO memory. Due to the slow connection to the computer, it first collects the data and dumps it into the SRAM. The FIFO memory also has limited space; for example, it can hold up to 1000 counts. If it exceeds this amount, it over flows. Therefore, this memory should not be allowed to fill up. After approximately 100,000 to 1 million measurements, it reads the SRAM memory from the beginning and sends it to the computer at a slower speed [14,18].

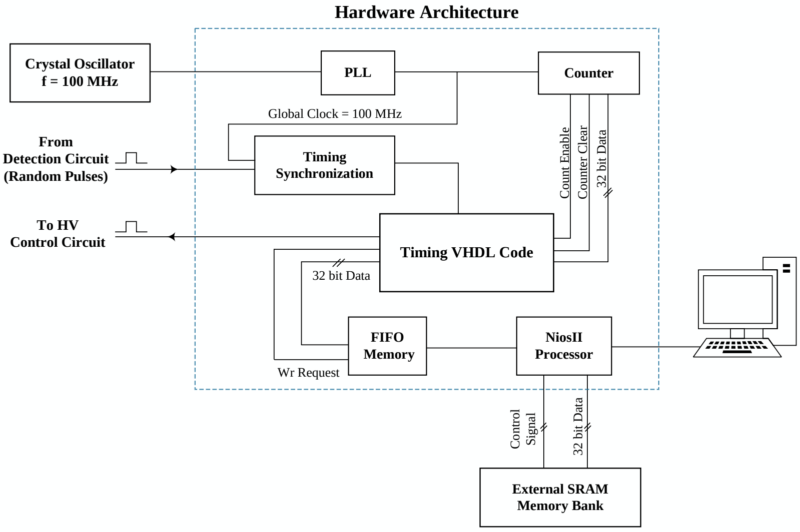

Fig. 2. Hardware structure, block diagram, and FPGA board communications.

3. Results and discussion

Nuclear processes often behave according to the Poisson distribution function. As a result, events in these processes occur more frequently at shorter intervals.

In Fig. 3, the ZP1210 detector with the active quenching circuit has measured thousands of time intervals. This figure shows that the accumulation intensity of the time intervals obtained from the circuit output of Fig. 1 is much higher for shorter time intervals.

Additionally, as the time interval on the vertical axis of the graph increases, the number of these points decreases. Thus, the measurement aligns with the Poisson distribution function.

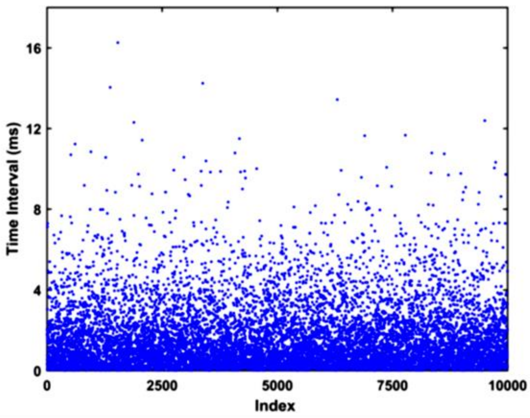

Fig. 3. Time interval diagram in terms of detector data distribution with active quenching circuit.

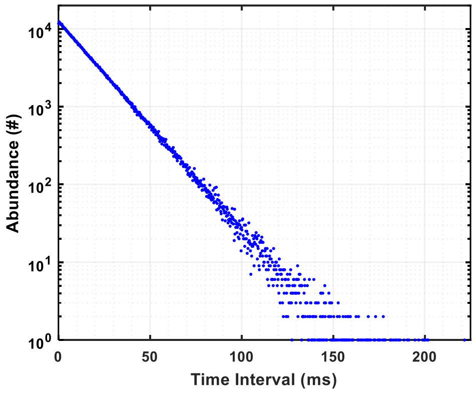

Fig. 4. Diagram of detector data abundance with an active quenching circuit in terms of time intervals.

The diagram in Fig. 4 shows the frequency ratio in terms of the time interval. As expected, higher frequencies are observed in shorter time intervals. Moreover, the probability distribution function is exponential. The logarithm of an exponential function is known to be linear. Therefore, in Fig. 3, the vertical axis is drawn logarithmically, resulting in a linear display. This confirms that the Poisson distribution function governing the nuclear process in this study is consistent with this behaviour.

Therefore, the accuracy and correct operation of the designed system are documented for the following two reasons:

A. The shorter the time interval, higher the likelihood of occurrence and accumulation of data.

B. The resulting linear logarithmic function indicates that the Poisson distribution function governing the process is exponential.

The images obtained from the output of the Geiger-Muller detector with active quenching in this study are shown on three oscilloscope channels as follows:

- Channel 1: Detector Signal
- Channel 2: Detected Pulse
- Channel 3: High Voltage Control Signal

Fig. 5 shows the time scale of these three signals in the range of -5µs to +5µs. In Fig. 6, this time range is extended to +125µs to -125µs.

In summary, the detector signal enters the Schmitt trigger and comparator circuit, converting it to a 3.3V LVTTL pulse. The signal then enters the FPGA, resulting in the high voltage control command exiting the FPGA.

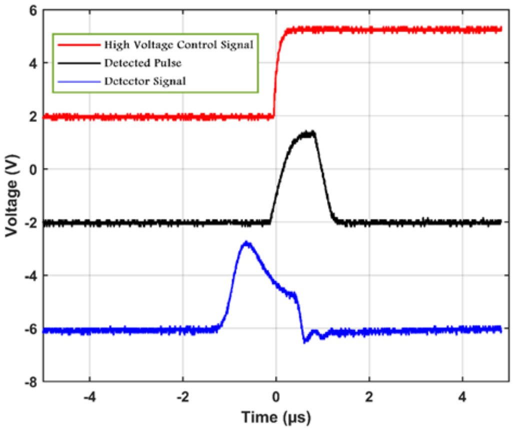

Fig. 5. Three output signals in 5µs time interval.

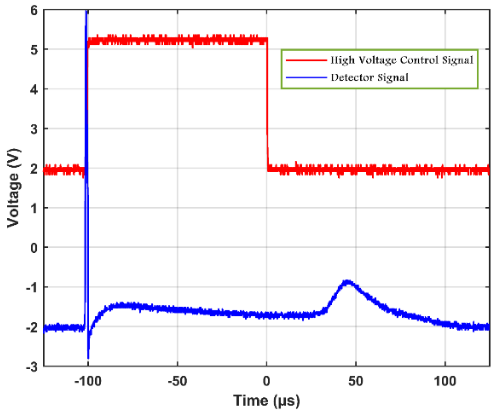

Fig. 6. Two output signals in 125µs time interval.

When a pulse is detected, the avalanche process occurs naturally; therefore, its high voltage value should be immediately lowered, eventually turning off and then switching on again.

The purpose of increasing the time scale in Fig. 6 is to observe the full high-voltage command signal, albeit with decreasing pulse width. The width of the control pulse (the high part of the signal) required to turn off the detector is about 100 microseconds. When the pulse is low, the detector activates and an avalanche occurs; as a result, the time base is the downward edge of the control pulse.

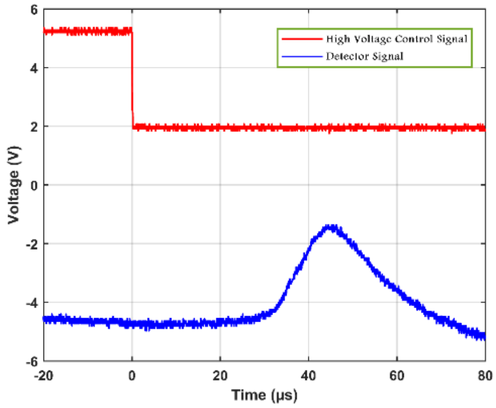

Fig. 7. Two output signals in a focused time interval to observe the fluctuation.

As shown in Figs. 5 and 6, when the high voltage value is changed by the control pulse of the high voltage switch, after about 45µs, a fluctuation (very low amplitude pulse) is observed on the detector signal. This is due to the capacitors in the detector inducing voltage. The high voltage value increases as the downward edge of the switch control signal is reached. Note that, based on radiation detection, the control signals are activated, and there is no constant period of the control or switching signals. In Fig. 7, the detector signal when the quenching circuit is inactive is shown. The pulse has two distinct parts: the first part is the fast rise with a high amplitude, and the second part is the exponential tail of the signal, which is relatively slow. Using the discriminator circuit shown in Fig. 1, the rise of the signal is detected and then is standardized for LVTTL using the HFE 40106 Schmitt trigger. The resulting triggering pulse is utilized by the FPGA to control the high voltage of the detector, enforcing the Geiger-Muller detector to be turned off (active quenching of the Geiger-Muller detector). The control signal and the high voltage power supply are shown in Fig. 8.

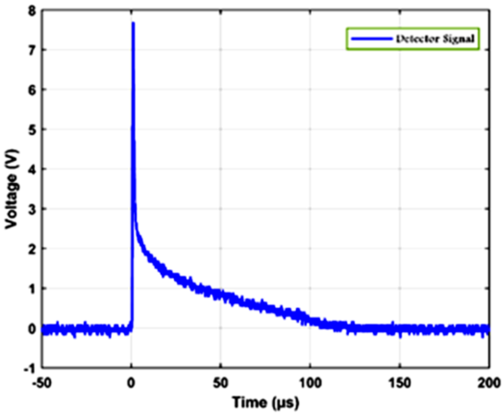

Fig. 8. Detector signal when the quenching circuit is inactive.

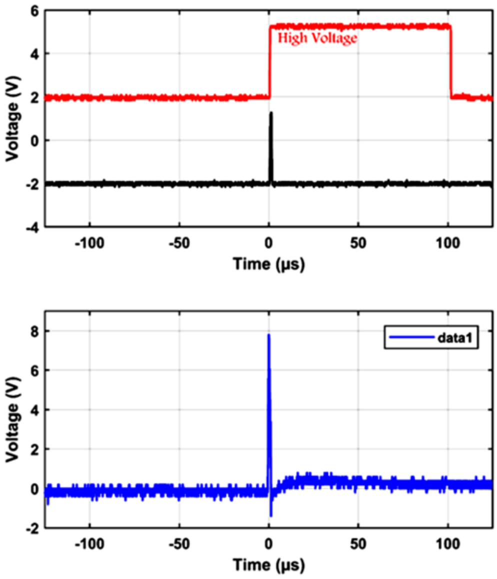

Fig. 9. Separating the detector signal from the two detected signals and the high voltage control signal.

Finally, by comparing the proposed active quenching circuit in this study (Fig. 9) and the designed active quenching circuit by Vagle et al. (Fig. 10), both of which are applied to the Geiger-Mueller ZP series 12, a clear difference in the reductions of their dead time can be seen. According to Fig. 10 (ZP1200, dead time: 90μs), with the activation of active quenching circuit, the output signal has a tail with a time interval of about 13 microseconds until reaching zero value and actually stopping the internal avalanche phenomenon of the detector. However, in Fig. 9 (ZP1210, dead time: 200μs) this time interval is about zero, which is significantly less than the reduced dead time of ZP1200. This significant difference demonstrates the validity and efficiency of the proposed circuit design.

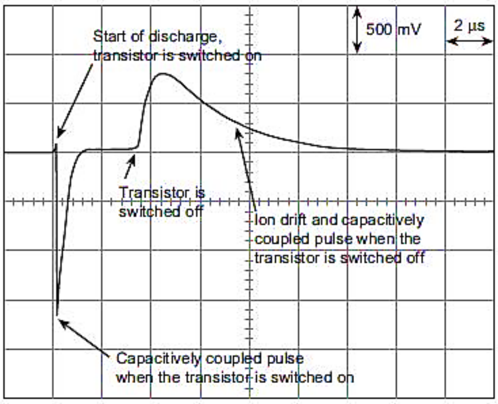

Fig. 10. Filtered amplifier output signal of active quenching circuit in ZP1200 GMT [10].

4. Conclusion

Geiger Muller detectors are widely used in the nuclear industry due to their simplicity of use and low-cost applications. Despite their competitive advantages, there are some drawbacks, such as lengthy dead time and limited lifetime (limited number of detection pulses). Depending on the size of the detector, the dead time ranges from several microseconds to few hundred microseconds. Every detection pulse consumes a quenching gas atom; therefore, the lifetime of the detector is limited due to the nature of the detector construction design. An effective method to reduce the dead time and extend the lifetime of the detector simultaneously, is utilization of active quenching systems although this adds complexity to the electronic circuitry.

In this work an active quenching system based on FPGA for ZP1200 Geiger-Muller detector is developed and tested in experimentally. The design is unique as as it employs FPGA technology. Both active quenching and data acquisition functionalities as well as data analysis, are implemented in the integrated design. By this approach, the physical aspects of the design (design circuitry) and power consumption (as the required electronic components are minimized) reduced, making it efficient for portable applications.

Reducing the dead time of a Geiger-Muller detection system is a crucial feature which is vitally important at high counting rates. For example, during a nuclear reactor accident, the radioactive material inventory of the reactor core might expose high dose rates that are much higher than its typical value during normal operation. As active quenching can extend the lifetime of Geiger-Muller detectors, this feature also is inherently embedded in the design compensating for the additional cost and complexity of the required electronic design.

Conflict of interest

The authors declare no potential conflict of interest regarding the publication of this work.

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